

**PENDING CLAIMS**

The following is a list of currently pending claims. No claims are added, cancelled, or amended in this response.

1. (Original) A thin film transistor comprising polysilicon, wherein the polysilicon is formed by a method comprising:
  - depositing a first layer of amorphous silicon;
  - depositing silicon nuclei on the first layer of amorphous silicon;
  - depositing a second layer of amorphous silicon over the first layer and the nuclei, wherein conversion of the first layer to hemispherical grains before deposition of the second layer is substantially prevented; and
  - annealing the first and second layers of amorphous silicon to induce crystallization.
2. (Original) The thin film transistor of claim 1, further comprising a charge storage region.
3. (Original) The thin film transistor of claim 2, wherein the charge storage region is ONO-type.
4. (Original) The thin film transistor of claim 2, wherein the charge storage region comprises a floating gate.
5. (Original) A monolithic three dimensional memory array comprising memory cells, said memory cells comprising polysilicon, any of said polysilicon crystallized by a method comprising:
  - embedding deposited silicon nuclei between layers of amorphous silicon; and
  - crystallizing from the embedded silicon nuclei.
6. (Original) The monolithic three dimensional memory array of claim 5, wherein the memory cells comprise TFTs.

7. (Original) The monolithic three dimensional memory array of claim 5, where the memory cells comprise antifuses and either diodes or diode components.
8. (Original) A thin film transistor comprising a channel region formed by a method comprising:
  - embedding deposited silicon nuclei between layers of amorphous silicon; and
  - annealing the nuclei and amorphous silicon layers.
9. (Original) The thin film transistor of claim 8, further comprising a charge storage region.
10. (Original) The thin film transistor of claim 9, wherein the charge storage region is ONO-type.
11. (Original) The thin film transistor of claim 9, wherein the charge storage region comprises a floating gate.